IN THE SPECIFICATION

Please amend the Title on page 1 as follows:

SEMICONDUCTOR DEVICE HAVING BURIED CONDUCTIVE LAYER FORMED IN AN INSULATING LAYER AND METHOD OF MANUFACTURING THEREOF

Please replace the paragraph at page 1, line 24 to page 2, line 4, with the following rewritten paragraph:

In order to solve the problem, the wiring resistance or the capacitance between the wiring lines is required to be reduced. Accordingly, wiring materials of low resistances and insulating film materials of low dielectric constants have been widely employed. For example, as the wiring materials, instead of aluminum (Al) heretofore used, copper (Cu) has been employed, resistivity of which is lower than that of aluminum by about 35 %. As the interlayer insulating film, SiOF films with relative dielectric constants k less than 3.6 or the like ~~has~~ have been employed, instead of SiO_2 films with relative dielectric constants k not less than about 4.1.

Please replace the paragraph at page 4, lines 9-20, with the following rewritten paragraph:

A method of manufacturing a semiconductor device according to a second aspect of the present invention includes forming a first interlayer insulating layer, forming a trench in the first interlayer insulating layer, forming a conductive layer on the first interlayer insulating layer to bury the conductive layer in the trench, and polishing a surface of a resultant structure after forming the conductive layer to form a flat surface in which the first interlayer insulating layer and the conductive layer are exposed. Thereafter, the method further includes etching a mechanically damaged layer, which is caused by the polishing and

remains on a surface of the first interlayer insulating layer. Furthermore the method includes forming an insulating film having a flat surface on the surface of the resultant structure after the etching, and forming a second interlayer insulating layer on the insulating film. The second interlayer insulating layer has a high etching selective ratio to the insulating film.

Please replace the paragraph at page 7, line 26 to page 8, line 3, with the following rewritten paragraph:

Next, description will be made on a method of manufacturing the semiconductor device according to the first embodiment with reference to Figs. 3A to 3E. Note that a method of forming the Cu wiring will be mainly described herein while omitting description on a formation step of [[a]] an element separation structure using a conventional method and a formation step of functional elements such as transistors.

Please replace the paragraph at page 11, lines 20-24, with the following rewritten paragraph:

Subsequently, as shown in Fig. 4C, the cap layer 90 is removed by etching with diluted hydrofluoric acid. As a result, the exposed surface of the first interlayer insulating layer 32 is lowered with respect to that of the Cu wiring 52 by a thickness of the removed cap layer 90. Moreover, a mechanically damaged layer due to the CMP process ~~dose~~ does not exist on the exposed surface of the first interlayer insulating layer 32.

Please replace the paragraph at page 13, lines 24-27, with the following rewritten paragraph:

Then, the surface of the resultant structure is to be ~~flatted~~ flattened by use of the CMP process. As a result, the anti-diffusion film 63 having a substantially flat surface as shown in

Fig. 5C can be formed. Specifically, the anti-diffusion film 63 can be formed to be thin on the Cu wiring 53 and to be thick on the first interlayer insulating layer 33.

Please replace the paragraph at page 14, lines 1-8, with the following rewritten paragraph:

Accordingly, a second interlayer insulating layer 73 is formed on the anti-diffusion film 63 ~~flatted~~ flattened similarly to the first and the second embodiments. Even if misalignment occurs in formation of necessary contact holes, since the anti-diffusion film 63 is formed to be thick in a portion of the contact hole other than the Cu wiring 53, the progress of etching can be sufficiently suppressed within the anti-diffusion film 63 even in the case of performing overetching. As the result, generation of a local deep portion in a contact hole is prevented, whereby a problem such as insufficient burying of the contact holes is prevented.

Please replace the paragraph at page 15, lines 7-12, with the following rewritten paragraph:

In the case of using the semiconductor manufacturing method according to the second embodiment, the wet etching step is first carried out for removing the cap layer after the CMP process. The subsequent steps are sequentially carried out until the annealing step of the second interlayer insulating layer. The subsequent steps are the same as those in the first embodiment, and are carried out under the atmospheric pressure, not requiring a high vacuum chamber.